IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

UNIRAM TECHNOLOGY, INC, **No C-04-1268 VRW**

Plaintiff, **ORDER**

v

MONOLITHIC SYSTEM TECHNOLOGY, INC, et al,

Defendants.
_____/

Plaintiff UniRAM Technology, Inc ("UniRAM") owns the two patents-in-suit, which relate to dynamic random access memory ("DRAM") and methods for the manufacture thereof. UniRAM contends that defendants Taiwan Semiconductor Manufacturing Company, LTD and TSMC North America (collectively "TSMC") and Monolithic System Technology, Inc ("MoSys") infringed UniRAM's United States Patent No 6,108,229 (the "'229 patent"). SAC (Doc #16-1). MoSys and TSMC separately denied the allegations and, on counterclaims, sought a declaratory judgment that both the '229 patent and UniRAM's United States Patent No 6,687,148 (the "'148 patent") were invalid,

unenforceable and not infringed. MoSys SAC Ans (Doc #23); TSMC SAC Ans (Doc #27).

On October 13, 2005, the court held a claim construction hearing for disputed terms in both patents pursuant to Markman v Westview Instruments, Inc, 517 US 370 (1996). Based on the parties' submission to the court and their arguments at the hearing, the court issues the following claim construction order.

As the court writes principally for the parties, it will not discuss the details of the inventions or define terms well-known to those skilled in the art, except as is necessary to construe the patent claims. Nor will the court recapitulate the parties' agreed-upon constructions, which can be found in the final joint claim construction statement. Jt Cl Const (Doc #117), Ex A.

I

The '229 patent, which issued on August 22, 2000, to Dr Jeng-Jye Shau ("Shau"), discloses a DRAM cell array that is manufactured by processes typically used to produce logic devices such as CPUs and microprocessors. The '148 patent, which issued on February 3, 2004, to Shau, discloses methods for manufacturing DRAM cell arrays by processes typically used for producing logic devices.

Although both patents have different claims, they share the same specification and stem from the same two patent applications. The '229 patent is a continuation-in-part both of application no 08/805,290 (issued United States Patent No 5,825,704) and application no 08/653,620 (issued United States Patent No 5,748,547). The '148 patent is a continuation of

application no 09/860,215 (issued United States Patent No 6,504,745), which in turn is a continuation-in-part of application nos 08/805,290 and 08/653,620, like the '229 patent. In short, the '148 patent is a "nephew" of the '229 patent.

All claims in the '148 patent were allowed after the patentee amended them in response to an office action rejecting the claims on enablement and written description grounds. All claims in the '229 patent were allowed after the patentee withdrew some in response to an office action requiring restriction of the patent to one invention.

II

The construction of patent claims is a question of law to be determined by the court. Markman v Westview Instruments, Inc, 517 US 370 (1996). The goal of claim construction is "to interpret what the patentee meant by a particular term or phrase in a claim." Renishaw PLC v Marposs SpA, 158 F3d 1243, 1249 (Fed Cir 1998). In doing so, the court looks first to the claim itself:

> The claims of the patent provide the concise formal definition of the invention. They are the numbered paragraphs which "particularly [point] out and distinctly [claim] the subject matter which the applicant regards as his invention." 35 USC § 112. It is to these wordings that one must look to determine whether there has been infringement. Courts can neither broaden nor narrow the claims to give the patentee something different than what he has set forth. No matter how great the temptations of fairness or policy making, courts do not rework claims. They only interpret them.

EI Du Pont de Nemours & Co v Phillips Petroleum Co, 849 F2d 1430, 1433 (Fed Cir 1988).

"The claims define the scope of the right to exclude; the claim construction inquiry, therefore, begins and ends in all cases with the actual words of the claim." Renishaw, 158 F3d at 1248. "The words used in the claim are viewed through the viewing glass of a person skilled in the art." Brookhill-Wilk 1, LLC v Intuitive Surgical, Inc, 326 F3d 1215, 1220 (Fed Cir 2003) (citing Tegal Corp v Tokyo Electron Am, Inc, 257 F3d 1331, 1342 (Fed Cir 2001)). "Absent a special and particular definition created by the patent applicant, terms in a claim are to be given their ordinary and accustomed meaning." York Prods, Inc v Central Tractor Farm & Family Ctr, 99 F3d 1568, 1572 (Fed Cir 1996). The court may, if necessary, consult a variety of sources to determine the ordinary and customary meaning of a claim term, including "the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art." Innova/Pure Water, Inc v Safari Water, 381 F3d 1111, 1116 (Fed Cir 2004).

The court begins its construction of claim terms by consulting intrinsic evidence of the meaning of disputed claim terms, which includes the claims, the specification and the prosecution history (if in evidence). Lacks Industries, Inc v McKechnie Vehicle Components USA, Inc, 322 F3d 1335, 1341 (Fed Cir 2003) (citation omitted). "If upon examination of this intrinsic evidence the meaning of the claim language is sufficiently clear, resort to 'extrinsic' evidence * * * should not be necessary." Digital Biometrics, Inc, v Identix, Inc, 149 F3d 1335, 1344 (Fed Cir 1998). "[I]f after consideration of the intrinsic evidence,

there remains doubt as to the exact meaning of the claim terms, consideration of extrinsic evidence may be necessary to determine the proper construction." Id. Although extrinsic evidence such as expert and inventor testimonies, dictionaries and learned treatises can shed useful light on the relevant art, extrinsic evidence is "less significant than the intrinsic record in determining the legally operative meaning of claim language." Phillips v AWH Corp, 415 F3d 1303, 1317 (Fed Cir 2005) (quoting C R Bard, Inc v United States Surgical Corp, 388 F3d 858, 862 (Fed Cir 2004)) (internal quotation marks omitted).

"[A] court may constrict the ordinary meaning of a claim term in at least one of four ways[:]" (1) "if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim in either the specification or prosecution history;" (2) "if the intrinsic evidence shows that the patentee distinguished [the] term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention;" (3) "if the term chosen by the patentee so deprives the claim of clarity as to require resort to the other intrinsic evidence for a definite meaning;" or (4) "if the patentee phrased the claim in step- or means-plus-function format," then "a claim term will cover nothing more than the corresponding structure or step disclosed in the specification, as well as equivalents thereto * * *." CCS Fitness, Inc v Brunswick Corp, 288 F3d 1359, 1366–67 (Fed Cir 2002) (internal citations and quotation marks omitted).

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Limitations from the specification, such as from a preferred embodiment, cannot be read into the claims unless expressly intended by the patentee. Teleflex, Inc v Ficosa North Am Corp, 299 F3d 1313, 1326 (Fed Cir 2002) ("The claims must be read in view of the specification, but limitations from the specification are not to be read into the claims."). And "a construction that excludes a preferred embodiment 'is rarely, if ever, correct.'" C R Bard, 388 F3d at 865 (citing Vitronics Corp v Conceptronic, Inc, 90 F3d 1576, 1583 (Fed Cir 1996)).

With these legal principles in mind, the court now construes the disputed claim language in the patents.

III

1. "logic circuit"

"Logic circuit" is used in claims 1 and 22 of the '148 patent. UniRAM contends that "logic circuit" means "a high performance circuit, distinct from the circuits found in a stand-alone memory device, whose primary design goal is the efficient performance of logic functions, such as a microprocessor or ASIC." Jt Cl Const, Ex B at 12. MoSys construes logic circuit as "[a] circuit outside of the memory array that performs some processing or controlling function." Id. TSMC adopts the even broader definition, "[a] circuit that performs processing or controlling functions." Id.

The court first observes that, consistent with UniRAM's proposed construction, a "logic circuit" is different from a "peripheral circuit." When discussing peripheral circuits, the '148 patent consistently refers to circuitry such as sense

amplifiers and decoders, which are outside the memory cells but within the memory device. See, e g, '148 patent at 2:19-21 ("Peripheral circuits such as sense amplifiers, decoders, and precharge circuits are depend[ent] upon memory cell pitch"), 7:12-14 ("Each memory bank needs to have a full set of peripheral circuits"). When discussing logic circuits, the '148 patent consistently refers to logic components outside of the memory device. See, e g, '148 patent at 2:62-64 ("high density memory device placed on the same chip as high performance logic circuits"), 3:6-7 ("contradicting requirements between logic circuits and memory devices"). Although peripheral circuits contain "logic" components, that does not make them "logic circuits." Instead, the '148 patent consistently treats logic circuits and peripheral circuits as separate and non-overlapping entities. See, e g, 21:48-49 ("the transistors used for peripheral circuits and logic circuits").

Nonetheless, UniRAM's proposed construction is problematic because it defines logic circuit at a level of detail that is unsupported by the specification. UniRAM imports limitations that the specification never discusses —— for example, the specification never mentions a microprocessor or ASIC. Moreover, the specification implicitly concedes that "logic circuits" are not necessarily high performance by using the phrase "high performance logic circuits." '148 patent at 2:63-64; see also Phillips, 415 F3d at 1314 (use of term "steel baffles" strongly implies that not all baffles are made of steel).

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Accordingly, the court adopts a blend of the parties' constructions —— a "logic circuit" is "a circuit outside of the memory device that performs some processing or controlling function." This construction distinguishes "logic circuits," which are outside of memory devices, with "peripheral circuits," which are within memory devices.

As a final matter, the court notes that the parties apparently want "logic circuit" and "logic-circuit" to share the same construction. Jt Cl Const, Ex B at 12. Because the term "logic-circuit" is only used on a few occasions and always as "peripheral logic-circuit," the court declines to construe separately the term "logic-circuit."

2. "peripheral logic-circuit"

Claim 1 of the '229 patent includes the term "peripheral logic-circuit." UniRAM propounds a construction similar to its proposed construction for "logic circuit," and argues that "a 'peripheral logic-circuit' is a type of 'logic circuit' (namely a 'peripheral' one)." UniRAM Br (Doc #91) at 17. In particular, UniRAM explains that "a 'peripheral logic-circuit' is simply a 'logic circuit' located outside of, but on the same substrate as, a memory circuit * * * thereby forming an embedded memory device." Id at 30. MoSys construes peripheral logic-circuit as "[a] circuit outside of the memory array that performs some processing or controlling function;" TSMC adopts the same construction but omits the word "some" and changes "function" to "functions." Jt Cl Const, Ex B at 13. Under UniRAM's construction, the '229 patent covers only embedded DRAM; under MoSys's and TSMC's constructions,

the patent covers both embedded and stand-alone DRAMs.

The court agrees with UniRAM that the '229 patent pertains to embedded, and not stand-alone, memory technology, and therefore, MoSys's and TSMC's proposed constructions for "peripheral logic-circuit" are incorrect. The specification never discusses stand-alone DRAM, but discusses embedded technologies at length. '229 patent at 2:41-3:24 (discussing the difficulty in prior art embedded DRAM manufacturing and the novel approach employed in the invention), 20:16-24 (discussing the advantages obtained according to this invention as "[c]omparing with current art embedded memory technologies, the present invention simplifies the manufacture technology by more than 30%"), 22:2-19 (discussing the transistor properties of prior art embedded technology), 24:31-52 (discussing novel design methods to reduce effect of higher leakage current for transistors in embedded technology). The patent title, field of invention and various invention objectives all refer to embedded memory. Id at cover (Title: "High Performance Embedded Semiconductor Memory Device * * *"), 1:15-19 (Field of invention: "The present invention relates * * * particularly to embedded memory devices * * *"), 3:36-44 (Invention objectives: "to manufacture [embedded device] without using complex manufacture technology * * * to make embedded DRAM to have the same performance as high-speed logic circuits * * * to improve yield and reliability of embedded memory products). Moreover, the theme of manufacturing the DRAM memory cell using standard logic technology appears throughout the specification. A memory cell manufactured in this way would likely be part of an embedded, not stand-alone, DRAM. Id at 5:11-12 ("process step to manufacture a DRAM memory

cell by adding one masking step to standard logic technology"), 17:48-52, 17:63-66, 19:48-65, 20:18-20 ("the procedures used to build the DRAM cell are existing procedures of standard logic technology, except one masking step and one plasma-etching step"), 20:29-32. The specification also discusses the simultaneous manufacturing of memory cells and logic circuits. A memory cell manufactured in this way would be a part of an embedded, not stand-alone, DRAM. Id at 21:41-44 ("The word line transistor (1402) in the memory cell of the present invention has the same properties and it is manufactured in the same time as the transistors used for peripheral circuits and logic circuits.").

Nonetheless, MoSys and TSMC argue that this court cannot import limitations from the specification based on the patent title, invention objectives, field of invention and disclosed embodiments. But this argument overlooks the court's duty to interpret claims in light of the specification. The Federal Circuit has described the balance between these competing interests:

> [The] balance turns on how the specification characterizes the claimed invention. In this respect, this court looks to whether the specification refers to a limitation only as a part of less than all possible embodiments or whether the specification read as a whole suggests that the very character of the invention requires the limitation be a part of every embodiment. For example, it is impermissible to read the one and only disclosed embodiment into a claim without other indicia that the patentee so intended to limit the invention. On the other hand, where the specification makes clear at various points that the claimed invention is narrower than the claim language might imply, it is entirely permissible and proper to limit the claims.

Alloc, Inc v ITC, 342 F3d 1361, 1370 (Fed Cir 2003) (internal citations omitted) (emphasis added). Here, the whole character of the invention is geared toward embedded technology. The patent title, field of invention, invention objectives and disclosed embodiments all relate to embedded, not stand-alone, DRAM. Accordingly, the court concludes that the claims in the '229 patent were directed only at embedded DRAM.

Nonetheless, UniRAM's proposed construction is problematic because, as with its proposed construction for "logic circuit," UniRAM defines peripheral logic-circuit at a level of detail that is unsupported by the specification. UniRAM once again imports limitations that the patent never discusses, such as the use of a microprocessor or ASIC.

Moreover, contrary to UniRAM's proposed construction, the specification teaches that "peripheral logic-circuit" encompasses both embedded logic circuits and peripheral circuits. When discussing threshold voltages and gate thicknesses, the specification states:

> **The word line transistor (1402) in the memory cell of the present invention has the same properties and it is manufactured in the same time as the transistors used for peripheral circuits and logic circuits.**

'229 patent at 21:41-44. Claim 1 of the '229 patent states in relevant part:

> **1. A DRAM (dynamic random access memory) cell array supported on a substrate comprising * * ***
>
> **said select-transistor-gate and said logic-circuit-gate having substantially a same thickness;**
>
> **said select-transistor for each of said memory cells having a select-transistor threshold voltage and each of said logic-transistors of said peripheral logic-circuit**

> having a logic-transistor threshold voltage wherein said select-transistor threshold voltage is substantially the same as said logic-transistor threshold voltage.

Id at 25:29-26:11. The comparison in the specification between the properties of a word line transistor and the properties of a transistor used for peripheral and logic circuits finds a parallel in the comparison in claim 1 between the threshold voltage/gate thickness of a select-transistor and the threshold voltage/gate thickness of a logic-transistor in a peripheral logic-circuit. This parallelism is reinforced by the specification that alternatively refers to the "word line transistor (1402)" as "select transistor 1402." Id at 17:53-57. The parallel use of "peripheral logic-circuit" and "peripheral circuits and logic circuits," demonstrates that the former term encompasses peripheral circuits. Because courts should not construe patent terms to exclude disclosed embodiments, C R Bard, Inc, 388 F3d at 865, the court concludes that "peripheral logic-circuit" includes both embedded logic circuits and peripheral circuits.

Having determined that the patents-at-issue only relate to embedded technology, and that "peripheral logic-circuit" includes both peripheral circuits and logic circuits, the court construes "peripheral logic-circuit" to mean "a peripheral circuit and/or embedded logic circuit."

3. "logic transistors"; "said logic transistors"

"Said logic transistors" appears in claim 21 of the '148 patent. UniRAM asserts that the term means "[t]he previously-identified transistors designed and optimized to serve a logic function." MoSys asserts that the term lacks antecedent basis and

hence the claim is indefinite. If construed, however, MoSys and TSMC both contend that the term means the "transistors in a logic circuit." Jt Cl Const, Ex B at 18-19.

The construction of "said logic transistors" depends on the construction of "logic transistors." The court agrees with UniRAM that "said" merely means "previously identified." UniRAM Br at 31; id, Ex 21 at 6. Accordingly, the court first construes "logic transistors."

Throughout the specification, the patentee places adjectives in front of the term "transistor" to describe the function that the transistor has been designed to achieve. For example, the patent discusses "select transistors," which are designed to selectively activate the memory cell ('229 patent at 19:31-44); "storage transistors," which are capacitors designed for storing a binary bit (id at 19:45-47) and "isolation transistors," which are designed for isolating two adjacent logic transistors (id at 24:22-25). Applying this principle to "logic transistor," this term appears to describe a transistor that was designed and optimized to perform a logic function.

UniRAM's proposed definition for "said logic transistors" is function-based, which accords with how "logic transistor" is used in the patent. On the contrary, MoSys and TSMC's proposed definition is location-based, requiring "said logic transistor" to be within a logic circuit. This proposed construction conflicts with the specification, which states that logic transistors may be within memory cells: "[P]ractical memory devices using high performance logic transistor[s] in DRAM memory cells have been manufactured successfully." Id at 25:16-18. Because all parties

agree, and the court's earlier claim construction confirms, that logic circuits do not contain memory cells, defendants' location-based construction excludes this embodiment and hence is disfavored.

Nonetheless, MoSys asserts that the term lacks antecedent basis and is indefinite because this claim does not have a term "logic transistor" preceding "said logic transistor." UniRAM maintains that the antecedent phrase is "select transistor." UniRAM Br at 32 n16.

UniRAM's argument is bolstered by a passage in the specification of the '148 patent that teaches a method for manufacturing a DRAM cell array:

> (f) forming logic transistors on the substrate having polysilicon gates covered by an insulation protective layer; (f) [sic] connecting the gate of a plurality of the logic transistors to a ground voltage thus defining a plurality of isolation transistors each separating two adjacent logic transistors wherein the insulation protective layer of the isolation transistors and the adjacent logic transistors defining open areas therein-between * * * .

'148 patent at 24:25-32 (emphasis added).

Other than using "said" rather than "the," the originally-filed version of claim 21 exactly mirrored the above passage. The patent office objected to that claim because "logic transistor" was not shown in a diagram, and rejected the claim because the patentee had apparently failed to provide an adequate written description how logic transistors are formed on the substrate. Behun Decl (Doc #106), Ex C, Office Action dated 2/20/2003 for application 10/269,571 at 2 ¶¶ 1-2. In response, the patentee changed two references to "logic," corresponding to the

italicized words in the above passage, to "a plurality of select" and "select." Id, Office Action Response dated 8/20/03, at 7. The patentee explained that the amendments were done "to eliminate any claim related to the peripheral logic transistors. Instead, it is clearly defined as the select transistor of the memory cells, which is clearly shown and fully described all through the Specification." Id at 10-11.

A claim is not invalid for indefiniteness if its antecedent basis is present by implication. Cross Medical Products, Inc v Medtronic Sofamor Danek, Inc, 424 F3d 1293, 1319 (Fed Cir 2005). The passage and prosecution history show that "select transistors" and "logic transistors" are used interchangeably in claim 21, and thus, "select transistors" provides an antecedent basis for "said logic transistors." Accordingly, the court concludes that the term "said adjacent logic transistors" is not indefinite. The court adopts UniRAM's construction of "said logic transistors" as "the previously-identified transistors designed and optimized to serve a logic function."

4. "logic-transistor"

"Logic-transistor" only appears in claim 1 of the '229 patent. UniRAM proposes that the term means "a transistor designed and optimized to serve a logic function;" MoSys proposes "[a] transistor in a peripheral logic-circuit;" and TSMC contends that this term requires no construction, but if construed, it means "a transistor in a logic circuit." Jt Cl Const, Ex B at 13.

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The court observes that the patents use the terms "logic-transistor" and "logic transistor" interchangeably. See, e g, '229 patent at 23:20-23 ("applying substantially same implant processes in forming the select-transistor and the logic-transistors wherein the select-transistor and the logic transistors having substantially a same threshold voltage." (emphasis added)). UniRAM and TSMC do not seem to think that the hyphen matters. Their proposed constructions for this term are in essence identical to their proposed constructions for "said logic transistor." Jt Cl Const, Ex B at 13, 18-19. This strongly suggests that the court should adopt the same construction for logic-transistor that was adopted for "logic transistor."

Moreover, there is no need to insert a location-based component into the definition for "logic-transistor," because the one claim in which this term appears already specifies that the "logic-transistor" is within a peripheral logic-circuit. '229 patent at 25:29-26:11. Hence, MoSys's proposed construction that requires the logic-transistor to be within a peripheral logic-circuit is at best redundant. And TSMC's proposed construction that requires the logic-transistor to be within a logic circuit has no grounding in either the claim or in the specification. Accordingly, the court adopts UniRAM's proposed construction and defines "logic-transistor" as "a transistor designed and optimized to serve a logic function."

5. "said adjacent logic transistors"

The term "said adjacent logic transistors" is in claim 21 of the '148 patent. UniRAM asserts that this term means "logic

transistors adjacent to an isolation transistor." MoSys contends that the term is indefinite because it lacks antecedent basis, but to the extent it can be construed, MoSys agrees with TSMC that the term means "transistors in a logic circuit that are next to one another." Jt Cl Const, Ex B at 17.

As described above when construing "said logic transistor," "select transistor" provides an antecedent basis for "logic transistor" in claim 21. Accordingly, "adjacent select transistors" provides an antecedent basis for "said adjacent logic transistors." MoSys and TSMC's location-based construction requires the transistors to be in a logic circuit. For the reasons previously explained, the court rejects this construction. Moreover, even if defendants' construction were reformed to be no longer location-based, UniRAM's proposed construction better matches the language of claim 21, which states in part, "a plurality of isolation transistors each separating two adjacent select transistors." '148 patent at 27:46-48. Because "select transistor" and "logic transistor" are used interchangeably in claim 21, this phrase implies that logic transistors are separated by and adjacent to an isolation transistor. UniRAM's proposed construction best captures this meaning.

6. "typical transistor of a logic circuit"

Because transistors are well-known to persons of ordinary skill in the art and because the court has already construed "logic circuit," there is no remaining ambiguity in this term and no need to construe it at this time.

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7. "Gate"

"Gate" appears in claims 5, 12, 13 and 21 of the '148 patent. UniRAM asserts that "gate" should mean "gate electrode." Jt Cl Const, Ex B at 11. MoSys and TSMC, without providing any reason, contend that the term is indefinite; to the extent the term can be construed, they contend it means "polysilicon gate electrode." Id; TSMC Br (Doc #99) at 32; MoSys Br (Doc #103) at 53-54. Because the patentee expressly modified "gates" with "polysilicon" in claim 21 of the '148 patent, not all "gates" must be made of polysilicon. See Phillips, 415 F3d at 1314. Accordingly, the court adopts UniRAM's definition of gate as "gate electrode."

8. "WL-transistor gate"

"WL-transistor gate" appears in claim 13 of the '148 patent but does not appear in the specification except in a section paraphrasing the claim. '148 patent at 23:66-24:35. UniRAM contends that it means "the gate electrode in a memory cell transistor, which is connected to the word line (WL)." Jt Cl Const, Ex B at 31. MoSys and TSMC, again without providing any reason, contend that the term is indefinite; alternatively, they assert that the term means "the polysilicon gate electrode of the select transistor." Id.

As demonstrated presently, because "WL-transistor gate" is "amenable to construction," the term is not indefinite. Exxon Research and Engineering Co v United States, 265 F3d 1371, 1375 (Fed Cir 2001). The court rejects UniRAM's construction because it introduces the term "memory cell transistor," which is not

mentioned anywhere in the patent. MoSys and TSMC's proposed construction better accords which claim 13, which states in part: "word-line (WL) select transistors each having a WL-transistor gate * * *." '148 patent, at 27:1-3. In construing "gate," the court rejected defining that term using "polysilicon." The court therefore adopts a modified version of MoSys and TSMC's construction and defines "WL-transistor gate" as "the gate electrode of the word-line select transistor."

9. "field oxide"

All three parties offer different definitions of "field oxide." UniRAM's proposed definition is "oxide that physically and electrically isolates active areas." Jt Cl Const, Ex B at 8. TSMC adds in the requirement that the field oxide must be "grown;" MoSys contends that the field oxide must be "grown" and "thick." Id.

Although the patent often uses field oxide to define a trench capacitor's edges, field oxide formation is only described once: "The first step is to define active area 1502, and grow isolation field oxide 1504 to separate those [sic] active area." '229 patent at 19:50-52. This intrinsic evidence indicates that the field oxide is isolated and is "grown." But this passage is one of many that describes alternative manufacturing procedures for the invention. Id at 19:52-21:4. Limiting field oxide to that which is "grown" would improperly import limitations from the specification to the claim. Phillips, 415 F3d at 1323.

Moreover, there is no intrinsic evidence suggesting that the field oxide must be "thick." Accordingly, the court adopts UniRAM's proposed construction.

10. "field oxide layer"

Having construed "field oxide," the court sees no reason to construe "field oxide layer," because the parties do not disagree over the meaning of "layer."

11. "active area"

"Active area" appears in claims 3 and 4 of the '229 patent and claims 3, 4, 5, 6, 24 and 25 of the '148 patent. MoSys and TSMC assert that "active area" is defined as "[t]he area where the claimed select transistor and the trench capacitor are formed, that area being bounded by the edges of the field oxide layer." Jt Cl Const, Ex B at 1. UniRAM contends that the active area is the "area bounded by the field oxide layer." Id.

The court adopts UniRAM's construction because it is simpler and more accurately reflects the disclosed embodiments. For example, one problem with MoSys and TSMC's definition is that the specification does not clearly delineate the select transistor gate's boundary. The specification states, "[T]he poly silicon word lines 1606 define the gates of the select transistors * * *." '229 patent at 20:12-14. But Figure 15(c) shows these word lines traveling both in the active area 1502 and in the field oxide 1504. Because the specification never limits the gates to the active area, the select transistor gate could spill into the field oxide, making MoSys and TSMC's definition inaccurate.

More importantly, the complexity of MoSys and TSMC's construction is unnecessary, because the specification defines active area clearly and in concise terms: "The first step is to define active area 1502, and grow isolation field oxide 1504 to

separate those [sic] active area * * *." Id at 19:50-52. And in seven of the eight claims in which active area appears, it is as "active area isolated and defined by edges of a field oxide layer," "active area isolated by a field oxide," "active area isolated by said field oxide" or "active area isolated as an enclosed area by said filed [sic] oxide." Id at 26:16-17, 26:22-23 (claims 3 and 4); '148 patent at 25:55, 25:64-65, 26:9-10, 28:20-21, 28:26-27 (claims 3, 4, 5, 24 and 25). UniRAM's proposed construction captures this meaning better than MoSys and TSMC's construction.

12. "SRAM (static random access memory)"

Because SRAM is a term well-known by persons of ordinary skill in the art, the court declines to construe it at this time.

13. "surrounding"

The term "surrounding" appears only in claim 15 of the '148 patent. UniRAM asserts that the term means "encircling, in whole or in part." Jt Cl Const, Ex B at 26. MoSys contends that the term means "completely enveloping." Id. TSMC believes the term does not need any construction, and to the extent it does, TSMC supports MoSys's construction. Id.

The court adopts UniRAM's construction. First, it is not clear from claim 15 itself which definition is correct; the claim states in part, "forming a diffusion layer surrounding said trenches * * *." '148 patent at 27:14. Moreover, the one time the specification refers to "surrounding," it does little more than paraphrase the claim. Id at 24:20-23. Nonetheless, the use of "diffusion layer" at other points in the specification is

instructive: "This constraint can be removed if a diffusion layer (1805) is deposited around the trench capacitor (1802) as illustrated by the cross-section diagram in FIG. 18(a)." Id at 21:18-21. Figure 18(a) shows a cross-section of an embodiment in which the diffusion layer encircles a trench capacitor but does not "completely envelop" it. Id at fig 18(a). Hence, the court rejects MoSys's construction because it is too narrow to accommodate this embodiment, and adopts UniRAM's construction, which better accords with the specification.

14. "trench[es]"

The term "trench" appears in three '229 patent claims as part of "trench capacitor" and in eleven '148 patent claims as part of "trench capacitor," "capacitor trench," "trench mask" and "said trench[es]." Three different constructions are offered for "trench[es]." UniRAM proposes that "trench[es]" means "a recess in the surface of a substrate." Jt Cl Const, Ex B at 29-30. TSMC requires that this recess be "deep," and MoSys additionally requires that the recess be in the "active area" of the substrate and that "the initial etching into the substrate is nearly perpendicular to the substrate surface." Id.

At no point do the claims or specification suggest that the initial etching must be nearly perpendicular. Moreover, the patents never indicate that the trench must be deep. On the contrary, the specification suggests that the storage capacitor for the invention is smaller than that of prior art DRAM cells. '229 patent at 4:15-19, 17:46-50. Moreover, although MoSys and TSMC assert that figures 16(d) and 18(a) depict deep trenches, "the mere

fact that the patent drawings depict a particular embodiment of the patent does not operate to limit the claims to that specific configuration." Anchor Wall Systems, Inc v Rockwood Retaining Walls, Inc, 340 F3d 1298, 1306-07 (Fed Cir 2003).

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Accordingly, the court adopts UniRAM's definition of "trench[es]" as "a recess in the surface of the substrate."

15. "trench capacitor"

"Trench capacitor" appears in three claims in the '229 patent and nine claims in the '148 patent. The parties briefed this term together with the term "trench." The issue is whether a trench capacitor is formed wholly or partially within a trench. UniRAM argues that a trench capacitor includes a lateral component that is outside of the trench and connects to a transistor. UniRAM Br at 45. MoSys and TSMC instead contend that the lateral component is not part of the trench capacitor, which they assert must be formed wholly within the trench. MoSys Br at 43; TSMC Br at 33, n22. MoSys also asserts that UniRAM's proposed construction is too broad and includes non-trench capacitors such as a stacked capacitors, which only have a small portion within a shallow recess in the substrate. MoSys Br at 42-43.

The court agrees with MoSys and TSMC that a "trench capacitor" does not include the lateral components. In a section beginning with the "following advantages are obtained according to this invention," the patent states that "three edges of the trench capacitor are defined by field oxide" and the fourth edge "is defined by mask." '229 patent at 20:24-29. Accordingly, the trench capacitor cannot include the lateral components, which lie on top of the field oxide and do not share the same four edges as the trench. Figs 14(g), 18(b). And although the court does not limit the term "trench capacitor" to this particular embodiment, the court notes that the patent does not clearly indicate that a trench capacitor includes components outside of the trench. Moreover, UniRAM's broad definition creates ambiguity because the boundaries between the trench, lateral components and top electrode are unclear. Accordingly, the court adopts a modified version of TSMC's definition of "trench capacitor" that fits with the construction of "trench" above: "A capacitor formed entirely within a recess in the surface of a substrate."

16. "said capacitor trench"

"Said capacitor trench" is used once in claim 6 of the '148 patent and was not briefed separately by the parties. Because "said" is commonly used to refer to previously-identified elements, "said capacitor trench" is properly construed as "previously-identified capacitor trench."

But what is problematic is that "capacitor trench" was never previously used in claim 6 or in independent claim 2 on which claim 6 is dependent. Although claim 2 describes the step of

"applying a capacitive-transistor trench mask for etching a plurality of trench capacitors * * *," '148 patent at 25:45-50, it is unclear how this phrase provides an antecedent basis for "said capacitor trench." Does "said capacitor trench" implicitly define the trench within which the previously-mentioned "trench capacitors" were formed? Or is the patentee referring to the "trench capacitors" themselves? The specification provides no guidance to the court because the term "capacitor trench" is only used once in a section that paraphrases the claims. Id at 23:15-65. And UniRAM has not provided any guidance either —— UniRAM's briefs do not address this term, and in the joint claim construction statement, UniRAM directs the court to its non-existent discussion of "capacitor trench." Jt Cl Const, Ex B at 18. Accordingly, the court agrees with MoSys that the lack of antecedent basis for "said capacitor trench" renders that term indefinite.

17. "threshold voltage"

The term "threshold voltage" appears in claim 1 of the '229 patent and claims 1 and 22 of the '148 patent. MoSys and TSMC contend that threshold voltage should be defined in terms of a specified current that operates under normal conditions. Jt Cl Const, Ex B at 27. UniRAM instead defines threshold voltage as the critical gate electrode to source electrode voltage that turns on the transistor. Id.

Contrary to MoSys's and TSMC's proposed construction, the specification never discusses how threshold voltage depends on current flow or operating conditions. But the specification does

discuss "[t]he threshold voltage of those depletion mode transistors" in the context of activating those transistors with gate select and drain select signals. '229 patent at 16:57-17:34. Because this intrinsic evidence is more consistent with UniRAM's construction, the court defines threshold voltage is "the critical gate electrode to source electrode voltage that determines whether a field effect transistor is on or off."

18. terms with "substantially"

Five disputed terms contain "substantially:" (1) "said select-transistor threshold voltage is substantially the same as said logic-transistor threshold voltage," (2) "said select-transistor-gate and said logic-circuit-gate having substantially a same thickness," (3) "substantially a same [thickness]," (4) "substantially the same [threshold voltage]" and (5) "substantially all memory read errors." Jt Cl Const, Ex B at 19-22, 23-25. These terms appear in claims 1 and 5 in the '229 patent and claims 1, 13, 14, 22 and 26 in the '148 patent. The court only construes the term "substantially" in each of these phrases because the other terms either are construed elsewhere in this order or are agreed upon by the parties.

For all terms except "substantially all memory read errors," UniRAM contends that "substantially" means "approximately, but not necessarily exactly." MoSys and TSMC instead propose that substantially means "identical except for differences that would necessarily result from the transistors being manufactured at the same time using the same process." Id.

For "substantially all memory read errors," UniRAM proposes a definition of "approximately all, but not necessarily all, memory read errors." Id at 25. MoSys's proposed construction is "[t]he number of read errors that an error code checking (ECC) and correction means of the prior art could correct." Id. TSMC asserts that this term does not need any construction, but if construed, TSMC proposes the same definition as MoSys but with "memory checking" replacing "error code checking (ECC)." Id. Neither MoSys nor TSMC provide any arguments in support of their proposed construction of this term.

Other than one section of the specification in which the claims are simply paraphrased, the specification uses "substantially" only once, stating "[t]he sense amplifier used in the present invention is substantially the same as typical sense amplifiers used in the prior art." '229 patent at 11:33-35. UniRAM's construction of "substantially" is consistent with this use of the term, unlike MoSys's and TSMC's proposed constructions.

Nonetheless, both MoSys and TSMC contend that their proposed constructions mimic the specification, which provides many embodiments that teach simultaneously fabricating the select and logic transistors. '229 patent at 21:41-44, 23:10-23. But by importing this limitation from the specification, MoSys and TSMC are asking the court to limit the claims to particular embodiments, which is something that the Federal Circuit has admonished district courts not to do. Phillips, 415 F3d at 1323.

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MoSys also notes that UniRAM adopts language similar to MoSys's construction in UniRAM's Patent L R 3-1 disclosure. Id at 36-37. But this disclosure only addresses how MoSys allegedly infringes UniRAM's '229 patent. The disclosure does not address the scope of UniRAM's claims. In other words, UniRAM's particular description how MoSys infringes UniRAM's patent in this case does not mean that UniRAM is limited to that description in all cases.

MoSys also argues that UniRAM's construction would render the claim indefinite because a standard for measuring "substantial" is required to provide notice to a person of ordinary skill what is covered by the claims. Id at 39-40. But the patents do provide some measure of what "substantially" means, albeit indirectly. UniRAM admits that it distinguished between threshold voltages of 0.7 and 1.1 volts, and oxide thicknesses of 70 and 100 angstroms. UniRAM Reply (Doc #118) at 19:18-28; '229 patent at 21:39-22:44. Accordingly, the difference between two threshold voltages or thicknesses necessarily cannot be greater than or equal

to 0.4 volts or 30 angstroms, respectively, if the two values are "substantially the same."

Because substantially is not defined explicitly in the patent and does not appear to carry any special meaning in the relevant field, the court turns to the term's customary and ordinary meaning. Schumer v Laboratory Computer Systems, 308 F3d 1304, 1311 (Fed Cir 2002) ("The proper approach is to construe the claim language using standard dictionary definitions, because here, the claims have no specialized meaning."). UniRAM's proposed constructions for "substantially" fit comfortably with the term's usage in the patent. These constructions also match the term's dictionary meaning. See, e g, Webster's Third New Intl Dictionary 2280 (1981) (substantial[ly]: "being that specified to a large degree or in the main"); Black's Law Dictionary 1428-29 (6th ed 1990) (substantially: "[e]ssentially; without material qualification; in the main; in substance * * *"). And because there is no reason to think that the patentee intended to use "substantially" differently in different contexts, UniRAM's consistent definition for that term is preferable to defendants' piecemeal approaches. Accordingly, the court adopts UniRAM's constructions for the terms containing "substantially."

19. "error code checking (ECC) and correction means"

"Error code checking (ECC) and correction means" appears in claim 5 of the '229 patent and claims 14 and 26 of the '148 patent. The parties agree that this term is a "means-plus-function" limitation based on 35 USC § 112(6), which requires this court to define the claimed functions and then to

identify the corresponding structure(s) in the specification. Versa Corp v Ag-Bag Intern Ltd, 392 F3d 1325, 1328 (Fed Cir 2004). The parties also concur on the claimed function "checking and correcting substantially all memory read errors within a threshold error-detection-and-correction time." UniRAM Br at 46; MoSys Br at 45; TSMC Br at 37.

But the parties disagree on whether the patent sufficiently describes a structure for the claimed function, and if so, what that structure is. UniRAM maintains that the corresponding structure is an "ECC circuit." TSMC and MoSys both contend that the term is indefinite, but to the extent the term can be construed, MoSys asserts that it should be limited to the ECC structure illustrated in figure 20(b). Jt Cl Const, Ex B at 6-8.

For a means-plus-function claim, "while it is true that the patentee need not disclose details of structures well known in the art, the specification must nonetheless disclose some structure. Stated differently, the testimony of one of ordinary skill in the art cannot supplant the total absence of structure from the specification." Default Proof Credit Card System, Inc v Home Depot USA, Inc, 412 F3d 1291, 1302 (Fed Cir 2005) (citation omitted). And "[a] structure disclosed in the specification qualifies as [a] 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." Id at 1298.

Here, UniRAM cannot identify any corresponding structure in the specification that justifies broadly construing "error code checking (ECC) and correction means" to encompass any ECC circuit. The specification states "[t]he ECC circuit is well known to the

art, so we do not discuss it in further details." '229 patent at 11:61-63. This disclosure provides no structure that can form the basis of a means-plus-function claim. And in any event, UniRAM has not linked this disclosure to the claimed function, so to grant UniRAM broad coverage here would ignore that the "duty to link or associate structure to function is the quid pro quo for the convenience of employing § 112, ¶ 6." Default Proof, 412 F3d at 1298.

Nonetheless, the court also disagrees with MoSys and TSMC, who assert that the term is indefinite. Both MoSys and TSMC admit that at least some structure is provided by figure 20(b), which is a "simplified block diagram of a memory device equipped with ECC protection circuits." MoSys Br at 45, n26; TSMC Br at 38. In particular, figure 20(b) provides a high-level block diagram showing data memory 2001, ECC parity data 2003, ECC parity tree 2005 and ECC correction logic 2007. '229 patent at figure 20(b). The accompanying discussion teaches how these elements operate, and how they relate to the claimed function. Id at 24:61-25:15 (e g, "In case there are corruption data, an ECC correction logic (2007) will find out the problem and correct the error so that the output data will be correct;" "When a memory device is equipped with an ECC circuit, it will correct most single-bit errors. As a result, the refresh time of the memory device is no longer dependent on the worst bit in the memory."). Hence, figure 20(b) discloses a structure that provides an adequate basis for the means-plus-function claim and that links to the claimed function. Accordingly, the court concludes that "error code checking (ECC) and correction means" corresponds to the ECC protection circuit

shown in figure 20(b), which includes ECC parity data 2003, ECC parity tree 2005 and ECC correction logic 2007.

20. "threshold error-detection-and-correction time"

"Threshold error-detection-and-correction time" appears in claim 5 of the '229 patent and claims 14 and 26 of the '148 patent. The specification never explicitly defines this term and only uses the term when paraphrasing the claims. '229 patent 23:4-9, 24:13-15, 24:50-53, 24:61-25:15. Both MoSys and TSMC contend that this term is indefinite; MoSys also asserts that to the extent the term can be construed, it means "the point at which the error correction scheme of the prior art can no longer overcome errors." Jt Cl Const, Ex B at 26; TSMC Br at 39-42. UniRAM proposes a highly-similar construction that defines the term as "the time past which the error correction scheme can no longer consistently and accurately correct errors." Jt Cl Const, Ex B at 26.

UniRAM's proposed construction is problematic because the "consistently and accurately" limitation is never mentioned in the specification. More importantly, UniRAM's construction seems indefinite because it adds a meaningless limitation to the claims. For example, after replacing "threshold error-detection-and-correction time" with UniRAM's proposed construction, each of the claims would read: "an error code checking [ECC] and correction means * * * for checking and correcting substantially all memory read errors within the time past which the error correction scheme can no longer consistently and accurately correct errors." The phrases "checking and correcting substantially all memory read errors" and "consistently and accurately correct errors" both refer

to an ECC's effectiveness. Accordingly, when used together, either the former or the latter phrase is superfluous. Because a limitation cannot be construed out of the claims, UniRAM's proposed construction cannot be correct. Texas Instruments v United States ITC, 988 F2d 1165, 1171 (Fed Cir 1993).

MoSys's proposed construction suffers from the same indefiniteness problem. The specification notes that "[t]he ECC circuit [used in this invention] is well known to the art, so we do not discuss it in further details." '229 patent at 11:61-63. Accordingly, the terms "an error code checking [ECC] and correction means * * * for checking and correcting substantially all memory read errors" and "the point at which the error correction scheme of the prior art can no longer overcome errors" both rely directly on the effectiveness of prior art ECCs.

But simply because UniRAM's and MoSys's proposed constructions are indefinite does not necessarily mean that the claim is "insolubly ambiguous" or that "no narrowing construction can properly be adopted." Honeywell Intl, Inc v ITC, 341 F3d 1332, 1338-39 (Fed Cir 2003) (quoting Exxon Research, 265 F3d at 1375). Rather, UniRAM's expert, Carl Sechen, notes that "threshold error-detection-and-correction time" likely relates to a memory cell's refresh time, which is the time period since data was last fully written to the memory cell. UniRAM Br, Ex 3 ¶¶ 190-93. By improving the capability of a memory cell to correct errors, an ECC circuit allows a memory cell to have a longer refresh time, Tecc, as compared to the refresh time if there were no ECC, Tmin:

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> When a memory device is equipped with an ECC circuit, it will correct most single-bit errors. As a result, the refresh time of the memory device is no longer dependent on the worst bit in the memory. Instead the device will * * * function until the errors are more than what the ECC mechanism can correct. The refresh time (Tecc) is therefore higher than Tmin as shown in FIG. 20(a).

'229 patent at 25:9-14.

Accordingly, the specification supports modifying MoSys's construction so that "threshold error-detection-and-correction time" means the "maximum refresh time beyond which the ECC and correction means can no longer overcome errors." Because this definition imports the concept of a refresh time, constructing the term this way does not render it superfluous as used in the claims.

IV

In sum, the court has construed many of the disputed terms of the '229 and '148 patents according to the intrinsic record and the patents' plain language. The court declined to construe some terms in these patents because their meaning was no longer ambiguous after the court had construed other related terms.

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Additionally, in a letter sent on December 13, 2005, UniRAM requested that this court schedule a case management conference to discuss scheduling of pretrial and trial dates. MoSys and TSMC did not respond to this letter. Accordingly, the parties are instructed to appear for a case management conference on April 11, 2006, at 9:00 AM, for pretrial and trial scheduling.

IT IS SO ORDERED.

VAUGHN R WALKER
United States District Chief Judge